XMODEL

The Best Way to Verify Analog Circuits in SystemVerilog

scientific analog

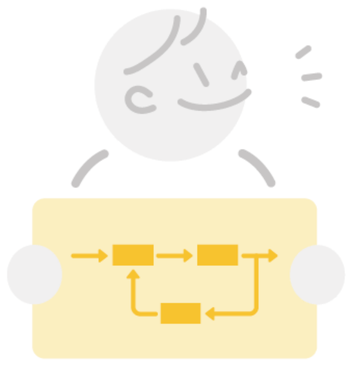
What's the Best Way to Verify My Analog Circuits in SystemVerilog?

Verification Engineers

I want to run faster simulation of analog models in SystemVerilog

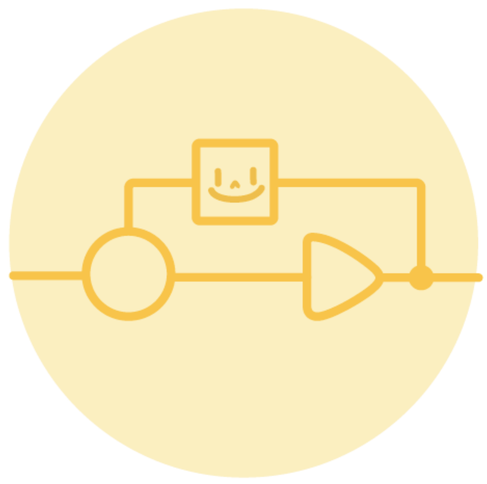
XMODEL is the fastest way to run analog simulation in SystemVerilog

Its unique event-driven algorithm and rich set of primitives make it easy to compose analog models that run 10~100x faster than Real-Number Verilog models.



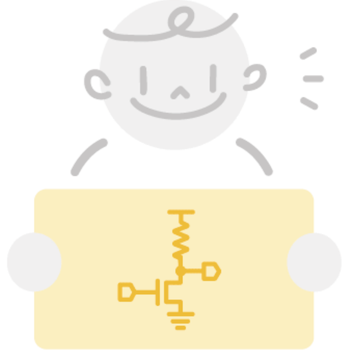
System Architects

I need to compose analog models but don't want to write codes



GLISTER lets you build top-down analog models in schematic forms

With GLISTER, writing analog models is simply drawing schematics with XMODEL primitive symbols in Cadence Virtuoso. No coding required!



Circuit Designers

I need to write SystemVerilog models for my analog circuits

MODELZEN can auto-extract bottom-up analog models from your circuits

With MODELZEN, you can automatically generate correct-by-construction, SPICE-accurate SystemVerilog models from your circuits just with a mouse click.

XMODEL

Analog/Mixed-Signal Models

XMODEL Primitives Library

SystemVerilog Simulator

XMODEL Simulation Engine

Simulation Results

Empower SystemVerilog with Event-Driven Analog Models

XMODEL is a plug-in extension to SystemVerilog that enables fast and accurate analog/mixed-signal simulation without SPICE. With its rich set of primitives, it is easy to compose both functional- and circuit-level analog models that run in an event-driven fashion entirely within System Verilog. Particularly, XMODEL offers the best way to verify your mixed-signal ICs with Universal Verification Methodology (UVM).

Fast and Accurate Analog Simulation in SystemVerilog

XMODEL uses revolutionary, patent-pending algorithms to express analog waveforms in equation forms and compute them efficiently in an event-driven manner. As a result, the SystemVerilog models composed with XMODEL primitives can achieve up to 10~100x speed-up compared to Verilog-AMS or Real-Number Verilog, without sacrificing accuracy.

XMODEL

Can be both fast and accurate thanks to fewer events

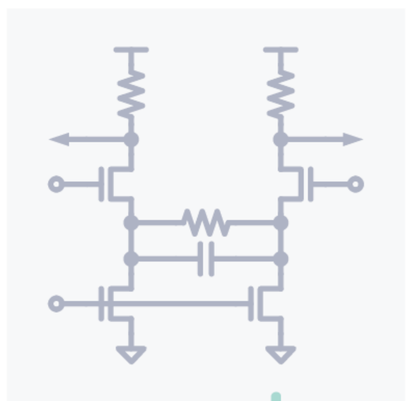
Other Simulators

SPICE, Verilog-AMS, Real-Number Verilog

Must trade speed for accuracy due to more events required

Circuit-Level Simulation in SystemVerilog

Currently, XMODEL is the only solution that enables true circuit-level simulation in SystemVerilog without invoking SPICE. Simply by listing the XMODEL's circuit-level primitives such as resistors, capacitors, transistors, and transmission lines, you can write analog models with loading effects, nonlinear behaviors, switching effects, and multiple drivers.



Circuit-Level Modeling

```
module ctle (
    output xreal outp, outn,
    input xreal inp, inn, vb, vdd, vss
);

xreal sp, sn;

nmosfet     #(.Kp(10e-3),.Vth(0.5))
            M1(.d(outn),.g(inp),.s(sp),.b(vss)),
            M2(.d(outp),.g(inn),.s(sn),.b(vss));
nmosfet     #(.Kp(5e-3),.Vth(0.4))
            M3(.d(sp),.g(vb),.s(vss),.b(vss)),
            M4(.d(sn),.g(vb),.s(vss),.b(vss));
resistor    #(.R(200))
            RL1(.pos(vdd),.neg(outp)),
            RL2(.pos(vdd),.neg(outn));
resistor    #(.R(10e3)) RC(.pos(sp),.neg(sn));
capacitor   #(.C(15e-15))
            CL1(.pos(vdd),.neg(outp)),
            CL2(.pos(vdd),.neg(outn));
capacitor   #(.C(30e-15)) CC(.pos(sp),.neg(sn));

endmodule
```

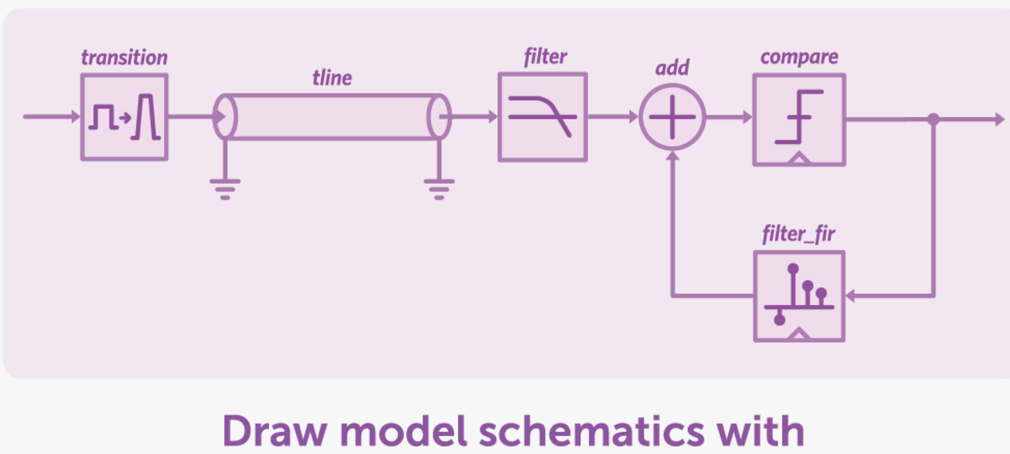
XMODEL-SPICE Co-simulation

The SystemVerilog models built with XMODEL primitives can also interface with SPICE netlists as well as Verilog-AMS or Real-Number Verilog models as supported by the host simulator.

Automate Simulations with XMULAN

XMULAN is an extensive Python library included in XMODEL. With XMULAN, you can write Python scripts that launch simulations while sweeping parameters, collect results, and post-process them.

GLISTER



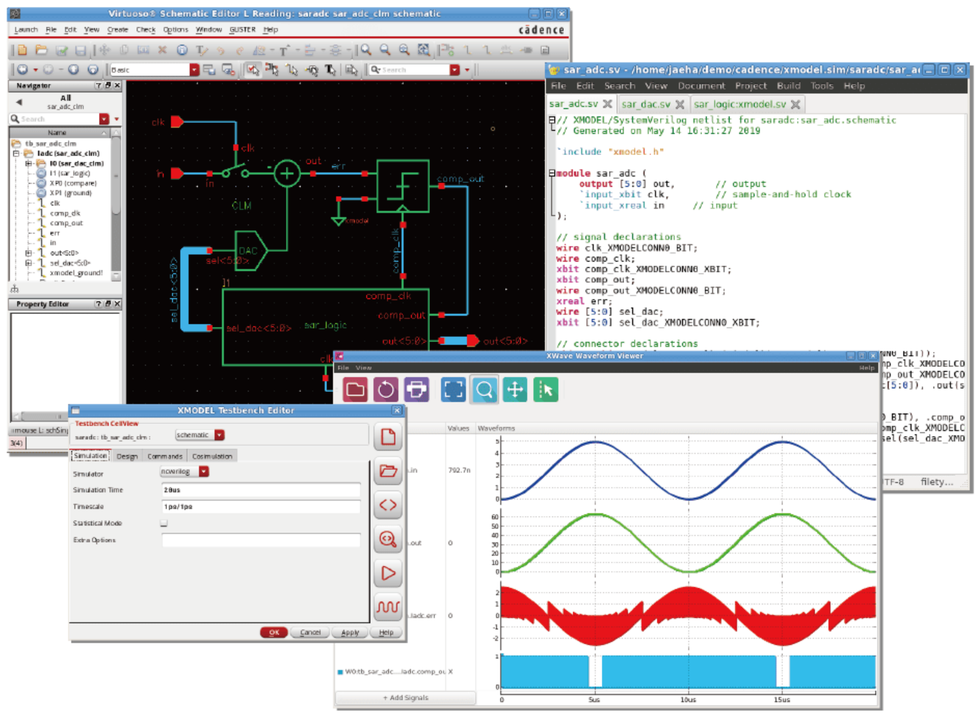
Draw model schematics with XMODEL primitive symbols

```
module dfe_trx (
    `output_xbit data_out,
    `input_xbit clk,
    `input_xbit data_in
);

xreal eq1, eq2;
xreal fb, rx, tx;

compare #(.threshold(0.0)) XP3 (.in_ref(`ground), .trig
transition #(.value1(1), .value0(0.0), .fall_time(0.0),
tline #(.Z0(50), .delay(0.0)) XP1 (.pos_2(rx), .neg_2(`
filter #(.zeros('{1.5e+08,0.0}), .poles('{5e+08,0.0,1e+
add #(.scale('{1,1}), .num_in(2)) XP5 (.out(eq2), .in({
filter_fir #(.data('{0.3,0.1}), .tran_time(0.0)) XP8 (.

endmodule
```

And GLISTER can netlist them into SystemVerilog models

Build Top-Down Analog Models in Schematic Forms

GLISTER is a graphical user interface for using XMODEL and MODELZEN within the Cadence Virtuoso Design Environment. With GLISTER, you can easily compose analog models in schematic forms and run XMODEL simulations without writing any codes.



Model Building with XMODEL Primitive Symbols

With GLISTER, writing models simply means placing the XMODEL primitive symbols on a schematic view and connecting them with wires. No coding is necessary! Also, the intuitive user interface friendly to analog designers makes analog modeling a breeze.

Mixed-Signal Hierarchical Netlisting

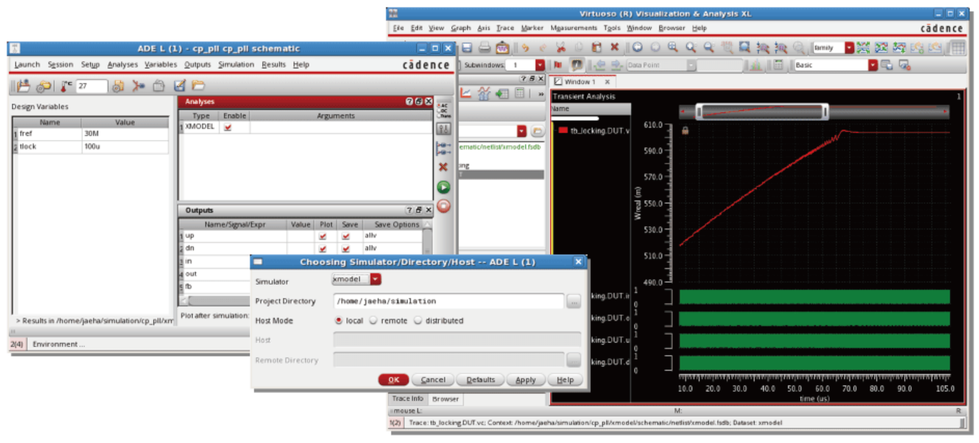
GLISTER understands that your schematic models may contain different types of signals connecting digital and analog components. GLISTER is the only SystemVerilog netlister that can automatically detect the type of each signal and insert type-coercing connectors as necessary.

Integrated Testbench Management

The GLISTER Testbench Editor provides a consistent interface for configuring testbenches, launching simulations, and viewing waveform results, as well as for preparing netlists and control files for XMODEL-SPICE co-simulation from a hierarchy configuration.

Integration with Cadence Analog Design Environment (ADE)

The GLISTER-ADE integration allows you to choose XMODEL as one of the supported simulators from the ADE sessions and perform key GLISTER tasks such as configuring testbenches, generating netlists, running simulations, and viewing waveforms, all using the familiar ADE menus and commands.



MODELZEN

Auto-Extract Analog Models from Circuits

With MODELZEN, automatic generation of analog models is not a dream; it's a reality! MODELZEN is a bottom-up model extractor that can translate any analog circuit into an equivalent System Verilog model using XMODEL primitives.

Quick, Correct-by-Construction Structural Model Generation

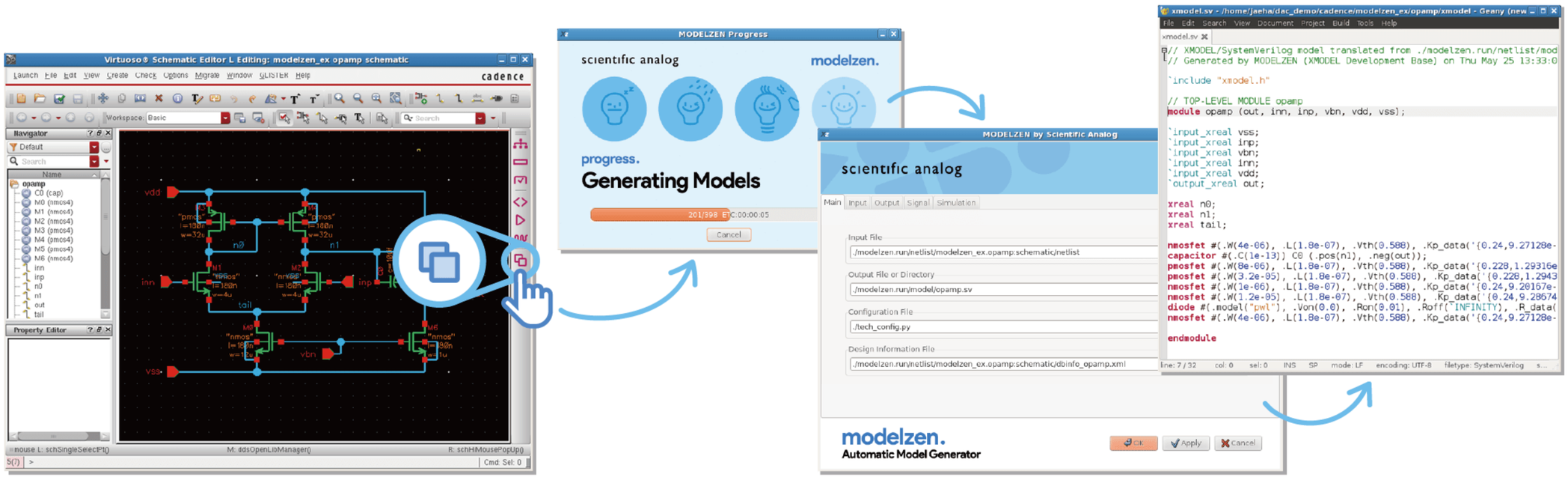
By default, MODELZEN generates structural models of the circuits, using the circuit-level primitives of XMODEL. In other words, MODELZEN builds models by first characterizing the individual devices composing the circuits and connecting the resulting device models according to the topology of the original circuits. This approach guarantees correct-by-construction models without requiring analog expertise and gets your full-chip models ready in just a few hours!

Functional Model Generation with User-Defined Models (UDMs)

In addition to circuit-level models, MODELZEN can also generate higher-abstraction models that enable faster simulation speeds. With the MODELZEN's new user-defined model (UDM) interface, you can map any selected parts of the circuits to custom functional models populated with SPICE-calibrated parameters. If you have been writing bottom-up models manually, the UDM interface is a great way to capture your expertise and automate the model generation flow.

Create Models from Circuit Schematics Just with a Mouse Click!

The GLISTER support for MODELZEN provides a user-friendly interface for generating SystemVerilog models directly from Cadence Virtuoso schematics. When initiated by a mouse click, GLISTER streamlines the whole steps of model generation with MODELZEN, including extracting circuit netlists, exporting MODELZEN properties, generating SystemVerilog models, and importing the models back to the design database.



About

Scientific Analog, Inc.

Scientific Analog, Inc. was founded in 2015 with a mission to make analog IC design as systematic and productive as digital. In particular, we believe that an effective use of analog models within the established digital flows is the key to successful design and verification of today's mixed-signal ICs.

XMODEL, GLISTER, and MODELZEN are our first line of products towards this mission. Currently, more than 40 companies and universities worldwide are using XMODEL.

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